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PTO/SB/50 (1/98)
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A/Reissue

jc564 U.S. PTO 11/11/99

jc511 U.S. PTO 09/438692 11/11/99

REISSUE PATENT APPLICATION TRANSMITTAL

Address to:
Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

Attorney Docket No.	3656US (95-0028RE)
First Named Inventor	Rodney C. Langley
Original Patent Number	5,686,762
Original Patent Issue Date (Month/Day/Year)	November 11, 1997
Express Mail Label No.	EL248174023US

APPLICATION FOR REISSUE OF: (check applicable box) [X] Utility Patent [ ] Design Patent [ ] Plant Patent

APPLICATION ELEMENTS

1. [X] * Fee Transmittal Form *(PTO/SB/56)* *(Submit an original, and a duplicate for fee processing)*
2. [X] Specification and Claims (*amended, if appropriate*)
3. [X] Drawing(s) *(proposed amendments, if appropriate)*
4. [X] Reissue Oath / Declaration (original or copy) *(37 C.F.R. § 1.175)(PTO/SB/51 or 52)*
5. Original U.S. Patent
   - [ ] Offer to Surrender Original Patent *(37 C.F.R. § 1.178)* *(PTO/SB/53 or PTO/SB/54)*
   - *or*
   - [ ] Ribboned Original Patent Grant
   - [ ] Affidavit / Declaration of Loss *(PTO/SB/55)*
6. Original U.S. Patent currently assigned?
   - [ ] Yes [ ] No
   - *(If Yes, check applicable box(es))*
   - [ ] Written Consent of all Assignees *(PTO/SB/53 or 54)*
   - [ ] 37 C.F.R. § 3.73(b) Statement [ ] Power of Attorney

ACCOMPANYING APPLICATION PARTS

7. [ ] Transfer drawings from Patent File
8. [ ] Foreign Priority Claim *(35 U.S.C. 119)* *(if applicable)*
9. [X] Information Disclosure Statement (IDS)/PTO-1449 [X] Copies of IDS Citations
10. [ ] English Translation of Reissue Oath/Declaration *(if applicable)*
11. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application, Status still proper and desired
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard *(MPEP 503)* *(Should be specifically itemized)*
14. [ ] Other: .....

**A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.*

15. CORRESPONDENCE ADDRESS

[ ] Customer Number or Bar Code Label *(Insert Customer No. or Attach bar code label here)* or [X] Correspondence address below

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Country	U.S.A.	Telephone	801-532-1922	Fax	801-531-9168

NAME (Print/Type)	Edgar R. Cataxinos	Registration No. (Attorney/Agent)	39,931
Signature		Date	11/11/99

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REISSUE APPLICATION FEE DETERMINATION RECORD	Docket Number (Optional) 3656US (95-0028RE)

Claims as Filed - Part 1

Claims in Patent	For	Number Filed in Reissue Application	(3) Number Extra	Small Entity Rate	Small Entity Fee		Other than a Small Entity Rate	Other than a Small Entity Fee
(A) 20	Total Claims (37 CFR 1.16(j))	(B) 29	**** 9 =	x $__ =		or	x $18 =	162.00
(C) 3	Independent Claims (37 CFR 1.16(i))	(D) 6	* 3 =	x $__ =			x $78 =	234.00
			Basic Fee (37 CFR 1.16(h))		$__			$ 760.00
			Total Filing Fee		$		OR	$ 1156.00

Claims as Amended - Part 2

	(1) Claims Remaining After Amendment		(2) Highest Number Previously Paid For	(3) Extra Claims Present	Small Entity Rate	Small Entity Fee		Other than a Small Entity Rate	Other than a Small Entity Fee
Total Claims (37 CFR 1.16(j))	***	MINUS	**	* =	x $__ =		or	x $__ =	
Independent Claims (37 CFR 1.16(i))	***	MINUS	*****	=	x $__ =			x $__ =	
				Total Additional Fee		$		OR	$

* If the entry in (D) is less than the entry in (C), Write "0" in column 3.
** If the "Highest Number of Total Claims Previously Paid For" is less than 20, Write "20" in this space.
*** After any cancelation of claims
**** If "A" is greater than 20, use (B -A); if "A" is 20 or less, use (B - 20).
***** "Highest Number of Independent Claims Previously Paid For" or Number of Independent Claims in Patent (C).

☐ Please charge Deposit Account No. _____ in the amount of _____
A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge any additional fees under 37 CFR 1.16 or 1.17 which may be required, or credit any overpayment to Deposit Account No. 20-1469 .
A duplicate copy of this sheet is enclosed.

☒ A check in the amount of $ 1156.00 to cover the filing / additional fee is enclosed.

November 11, 1999
Date

Signature of Applicant, Attorney or Agent of Record

Edgar R. Cataxinos
Typed or printed name

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SEMICONDUCTOR DEVICE WITH IMPROVED BOND PADS

FIELD OF THE INVENTION

The invention relates to semiconductor devices having bond pads for connection to an external circuit and, more particularly, to an improved bond bad having openings in the bonding surface of the bond pad.

BACKGROUND OF THE INVENTION

Many semiconductor devices utilize bond pads as the terminals for electrically connecting active circuits in the device to an external circuit. The bond pads are select areas of the interconnect wiring pattern left exposed after formation of the passivation layer which covers the semiconductor die. The active circuits in the die are connected to the interconnect wiring and accessed through the bond pads. Thin wires are bonded to the bond pads. These bond wires electrically connect the bond pads to metal leads which, after the die/lead assembly has been enclosed within a sealed package, are inserted into or otherwise attached to a printed circuit board.

During the wire bonding process, a heat block heats the die and the leads to a temperature of about 150° C. to 350° C. The end of the bond wire is heated by an electrical discharge or a hydrogen torch to a molten state, thus forming a ball of molten metal on the end of the bond wire. The molten ball is pressed by a bonding capillary tool against the heated bond pad, sometimes in combination with ultrasonic vibration, to alloy the metallic elements of the wire and the metal bond pad and thereby bond the wire to the pad. The bonding capillary tool is then moved to a bonding site on the appropriate lead. The wire is pressed against the heated lead to bond the wire to the lead. The bond wire is then tensioned and sheared. The process is repeated for each bond pad on the die.

The bonding surface of conventional bond pads is substantially flat. The present invention is directed in general to an improved bond pad and, more specifically, to a bond pad having openings formed in the bonding surface of the bond pad. It is believed that forming openings in the bonding surface of the bond pad may, in some instances, improve the strength of the wire bond.

SUMMARY OF THE INVENTION

Accordingly, it is one object of the invention to improve the strength of the bond between the bond wire and the bond pad formed during the fabrication of semiconductor devices.

It is another object of the invention to increase the surface area of the bond pad without also increasing the size of the bond pad.

According to the present invention, these and other objects are achieved by a semiconductor device that includes a bond pad electrically connected to an active circuit in the semiconductor device and at least one opening formed in the bonding surface of the bond pad. The opening(s) may include recesses extending partially into the bonding surface or channels that extend entirely through the bond pad. Various shapes and configurations of the openings may be used and tailored to specific device requirements. For example, the openings may be a pattern of rectangular channels disposed about the center of the bonding surface or an array of holes.

Additional objects, advantages and novel features of the invention will be set forth in part in the description that

follows, and in part will become apparent to those skilled in the art upon examination of the following or may be learned by practice of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a top down plan view of a bond pad having a series of rectangular channels arranged parallel to one another.

FIG. 2 is a cross section view taken along the line A—A in FIG. 1 wherein the openings extend through the bond pad.

FIG. 3 is a cross section view taken along the line A—A in FIG. 1 wherein the openings extend only partially into the bond pad.

FIG. 4–6 are top down plan views of alternative embodiments of the invented bond pad having various configurations of openings.

FIGS 7–9 are cross section views of the device of FIG. 1 at various stages of fabrication.

FIG. 10 is an expanded view of the bond between a bond wire and the bond pad of FIG. 1.

DETAILED DESCRIPTION OF THE INVENTION

FIGS. 1 and 2 are a top down plan view and a cross section view, respectively, of one of the preferred embodiments of the present invention. Referring to FIGS. 1 and 2, semiconductor device 10 can be any integrated circuit device, such as a random access memory (RAM), a programmable read only memory (PROM), a logic circuit or any type of application specific integrated circuit device. The active circuits (not shown), which are formed in a main region 12 of the semiconductor device 10, are electrically connected to bond pads 14. Bond pads 14 constitute select areas of a wiring pattern exposed through holes 16 in passivation layer 18. The wiring pattern and, correspondingly, bond pads 14 are formed on thick insulating layer 20. Openings 22 are formed in the bonding surface 24 of bond pads 14.

Preferably, openings 22 extend through bond pads 14, as shown in FIG. 1. Alternatively, openings 22 may be recesses that extend only partially into bonding surface 24, as shown in FIG. 3. Openings 22 comprise a series rectangular channels arranged parallel to one another as shown in FIG. 1. Other shapes and configurations may also be used and tailored to specific device requirements. For example, openings 22 may comprise a pattern of radiating channels disposed about the center of bonding surface 24 as illustrated in FIGS. 4, an array of L shaped channels as shown in FIG. 5, or an array of holes as shown in FIG. 6. To facilitate probing and testing, the center portion of bonding surface 24 may be left free of openings.

The openings are believed to promote a more robust bond by increasing the surface area available for bonding, but without increasing the size of the bond pad. In addition, it is believed that the sidewalls of openings 22 collapse during the bonding process, thereby further increasing bond strength.

The formation of semiconductor device 10 will now be described with reference to FIGS. 7–9. Semiconductor device 10 is formed using conventional fabrication processes and materials well known in the art, including etching predetermined patterns into the various layers of material. Such etching is referred to herein for convenience as "patterning and etching." Photolithography and reactive ion etching, for example, are commonly used pattern and etch

processes. These or other pattern and etch processes, well known to those skilled in the art, may be used to implement the present invention. Referring first to FIG. 7, active circuits (not shown) are formed in a main region 12 of semiconductor device 10. Thick insulating layer 20, typically made of phosphosilicate glass, is formed over the active circuits and usually extends into the periphery to cover the entire upper surface of the device. Insulating layer 20 is patterned and etched, and this etch may continue down through inferior layers of material, to open contact vias (not shown) to the active circuits. A layer of metal 26, typically aluminum, is deposited over insulating layer 20 and into the contact vias.

Referring now to FIG. 8, metal layer 26 is patterned and etched to form an interconnect wiring pattern. Preferably during this same pattern and etch step, openings 22 are formed in select areas of the wiring pattern at the desired locations of the bond pads 14. Referring to FIG. 9, passivation layer 18, typically made of phosphosilicate glass or silicon nitride, is then deposited over the entire surface of the device and patterned and etched to form holes 16 and thereby expose the select areas of the wiring pattern in which openings 22 were previously formed. Those areas of the wiring pattern exposed through holes 16 in passivation layer 18 constitute bond pads 14. For those embodiments of the invention wherein openings 22 extend through bond pads 14, a portion of the material comprising passivation 18 will typically be left in the bottom of the openings 22. If, and to what extent, such material remains in openings 22 will depend on the duration and selectivity of the passivation layer etch.

Referring to FIG. 10, bond wire 30 is bonded to bond pad 14. Bond wire 30 serves as an electrode for connection to an external circuit. As is known in the art, this wire bond connection is made by forming a molten ball on the end of bond wire 30 and pressing the molten ball against bond pad 14, which has been heated to a temperature 150° C. and 350° C., in the presence of ultrasonic vibration to alloy the metallic elements of bond wire 30 and bond pad 14. It is believed that the bonding process causes the sidewalls of openings 22 to collapse resulting in the bond shown in FIG. 10.

There has been shown and described a semiconductor device having an improved bond pad wherein openings are formed in the bond pad to help create a more robust bond between the bond pad and an electrode. The particular embodiments shown in the drawings and described herein are for purposes of example and should not be construed to limit the invention as set forth in the appended claims.

I claim:

1. A semiconductor device having an improved bond pad, the semiconductor device comprising:

a. a bond pad electrically connected to an active circuit in the semiconductor device;

b. a substantially flat bonding surface on the bond pad; and

c. an opening extending [partially into] <u>through</u> the bonding surface.

2. A semiconductor device according to claim 1, further comprising a plurality of openings in the bonding surface of the bond pad.

3. A semiconductor device according to claim 2, wherein the openings are disposed about a center portion of the bonding surface of the bond pad so the center portion of the bonding surface is free of openings.

4. A semiconductor device according to claim [4] 2, wherein the openings comprise a pattern of radiating channels disposed about a center of the bonding surface.

5. A semiconductor device according to claim 2, wherein the openings comprise a series of spaced apart rectangular channels arranged parallel to one another.

6. A semiconductor device according to claim 2, wherein the openings comprise an array of L shaped channels disposed about a center of the bonding surface.

7. A semiconductor device according to claim 2, wherein the openings comprise an array of holes disposed about the bonding surface.

8. A semiconductor device, which comprises:
a. an active circuit in the semiconductor device;
b. a wiring pattern overlying and in electrical contact with the active circuit;
c. bond pads formed as select areas on the wiring pattern; and
d. a plurality of openings extending [partially] into a substantially flat bonding surface of the bond pads.

9. A semiconductor device according to claim 8, wherein the openings are disposed about a center portion of the bonding surface of the bond pad so that the center portion of the bonding surface is free of openings.

10. A semiconductor device according to claim 8, wherein the openings comprise a pattern of radiating channels disposed about a center of the bonding surface.

11. A semiconductor device according to claim 8, wherein the openings comprise a series of spaced apart rectangular channels arranged parallel to one another.

12. A semiconductor device according to claim 8, wherein the openings comprise an array of L shaped channels disposed about a center of the bonding surface.

13. A semiconductor device according to claim 8, wherein the openings comprise an array of holes disposed about the bonding surface.

14. A semiconductor device according to claim 8, further comprising a passivation layer overlying the wiring pattern, the passivation layer having holes therethrough to expose the bonding surface of the bond pads to enable electrical connection to the bond pads through the holes.

15. A semiconductor device according to claim 8, further comprising bond wires bonded to the bonding surface of the bond pads.

16. A semiconductor device, comprising:
a. a layer of insulating material;
b. a substantially flat layer of conductive material over lying the layer of insulating material;
c. bond pads formed as select areas on a surface of the layer of conductive material; and
d. at least one opening extending [partially into] through the bond pads.

17. An improved bond pad comprising:

a metal layer having a substantially planar surface, said metal layer electrically connected to an active circuit of a semiconductor device and having at least one opening extending therethrough.

18. An improved bond pad according to claim 17, further comprising a plurality of openings in the metal layer of the bond pad.

19. An improved bond pad according to claim 18, wherein the openings are disposed about a center portion of the planar surface of the bond pad so that the center portion of the planar surface is free of openings.

20. An improved bond pad according to claim 18, wherein the openings comprise a pattern of radiating channels disposed about a center of the bond pad.

21. An improved bond pad according to claim 18, wherein the openings comprise a series of spaced apart rectangular channels arranged parallel to one another.

22. An improved bond pad according to claim 18, wherein the openings comprise an array of L shaped channels disposed about a center of the bond pad.

23. An improved bond pad according to claim 18, wherein the openings comprise an array of holes disposed about the bond pad.

24. An improved bond pad according to claim 18, further comprising a passivation layer overlying the metal layer, the passivation layer having holes therethrough to expose the planar surface of the bond pad to enable electrical connection to the bond pad.

25. An improved bond pad according to claim 18, further comprising a bond wire bonded to the planar surface of the bond pad.

26. An improved bond pad according to claim 18, wherein said metal layer is aluminum.

27. A semiconductor device having an improved bond pad, the semiconductor device comprising:

a bond pad electrically connected to an active circuit of the semiconductor device, said bond pad having a substantially planar surface; and

at least one opening extending through said bond pad.

28. A semiconductor device having an improved bond pad, the bond pad having a metal layer, said metal layer having a substantially planar surface connected to an active circuit of a semiconductor device further having at least one opening extending therethrough, the semiconductor device made according to the method comprising:

forming a thick insulating layer over active circuitry of a semiconductor chip;

etching said thick insulating layer thereby forming clear contact paths to said active circuitry of the semiconductor chip;

forming a metal layer over said thick insulating layer; and

etching said metal layer thereby forming an interconnect wiring pattern and bond pads having at least one opening extending therethrough.

29. A semiconductor device according to claim 27, the method further comprising:

forming a passivation layer over the metal layer; and

etching said passivation layer to expose select areas of the wiring pattern and bond pads.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Reissue Application of:

Rodney C. Langley

U.S. Patent No.: 5,686,762

Issued: November 11, 1997

For: SEMICONDUCTOR DEVICE WITH IMPROVED BOND PADS

Reissue Serial No.: To be assigned

Attorney Docket No.: 3656US(95-0028-RE)

NOTICE OF EXPRESS MAILING

Express Mail Mailing Label Number: EL248174023US

Date of Deposit with USPS: November 11, 1999

Person making Deposit: Jared Turner

REISSUE DECLARATION

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

The undersigned declarant, Rodney C. Langley, states and declares as follows:

My residence, post office address, and citizenship are as set forth at the end of this DECLARATION by my signature above my typed name.

I believe myself to be an original, first and sole inventor of the subject matter which is claimed and for which a reissue patent is sought on the invention entitled SEMICONDUCTOR DEVICE WITH IMPROVED BOND PADS, an application which was filed in the U.S. Patent and Trademark Office on December 21, 1995 and assigned Serial No. 08/577,911.

I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment specifically referred to in this DECLARATION, the amended originally issued claims 1-16 in U.S. Patent No. 5,686,762 and the amended claims 17-29 as first presented with this Reissue Application.

I acknowledge the duty to disclose to the Office all information known to me to be material to patentability as defined in 37 C.F.R. § 1.56.

Applicant believes the original patent to be partly inoperative or invalid by reason of the patentee claiming more or less than patentee had the right to claim in the patent.

Specifically, Applicant believes that the claims of the original application are too narrow in that product-by-process claims and claims to a bond pad were erroneously omitted from the original application. The patentee wishes to add these claims as per 35 U.S.C. § 251. The issue date of the original application was November 11, 1997, within the two year requirement of 35 U.S.C. § 251.

All errors which are being corrected in the present reissue application up to the time of filing of this declaration arose without any deceptive intention on the part of the Applicant.

I hereby appoint the following Registered Practitioners to prosecute this application and to transact all business in the Patent and Trademark Office:

Joseph A. Walkowski, Reg. No. 28,765
James R. Duzan, Reg. No. 28,393
Edgar R. Cataxinos, Reg. No. 39,931
Michael L. Lynch, Reg. No. 30,871
Lia M. Pappas, Reg. No. 34,095

I hereby direct that all correspondence and telephone communications be directed to Joseph A. Walkowski at TRASK, BRITT & ROSSA, P.O. Box 2550, Salt Lake City, Utah 84110, telephone (801) 532-1922.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: 11-11-99

Rodney C. Langley

Rodney C. Langley

Inventor's Full Name: Rodney C. Langley
Country of Citizenship: United States of America
Residence Address: 5930 W. Hollilynn
Boise, Idaho 83707

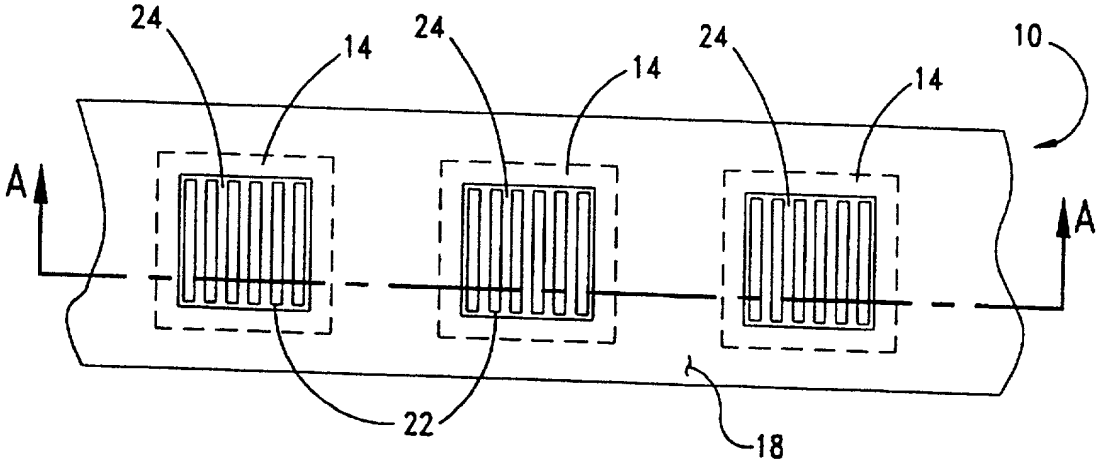
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FIG. 1

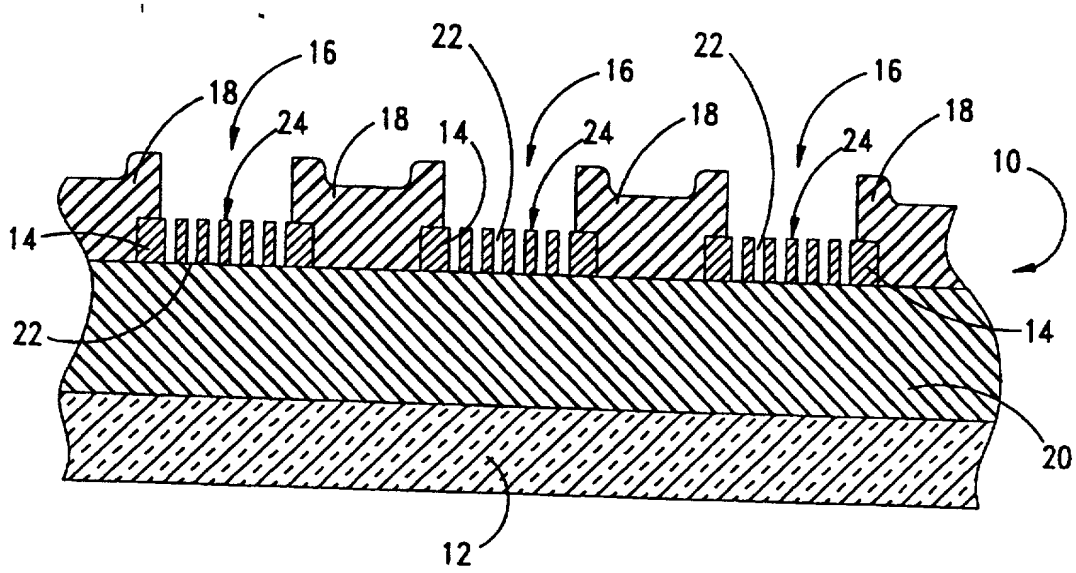
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FIG. 2

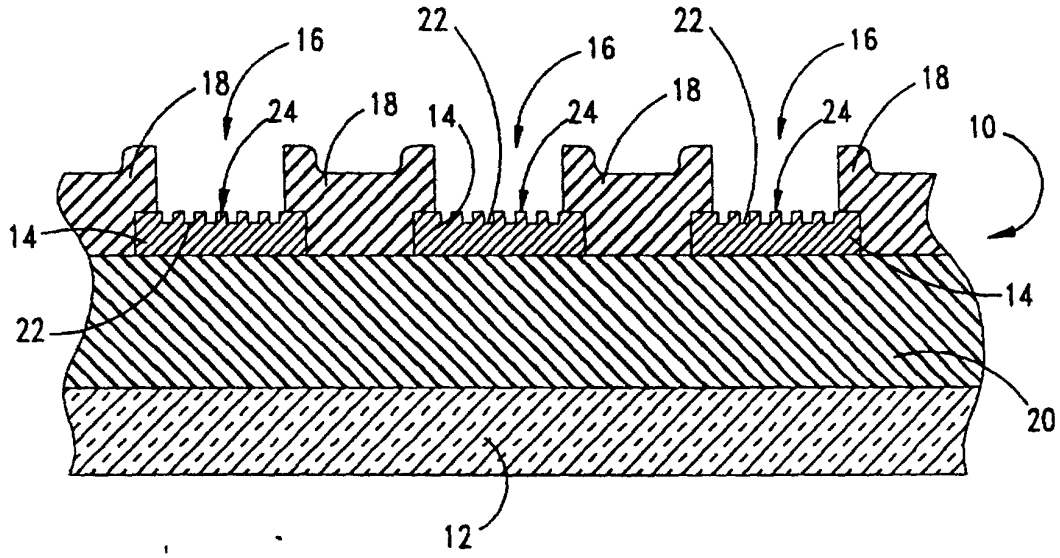

FIG. 3

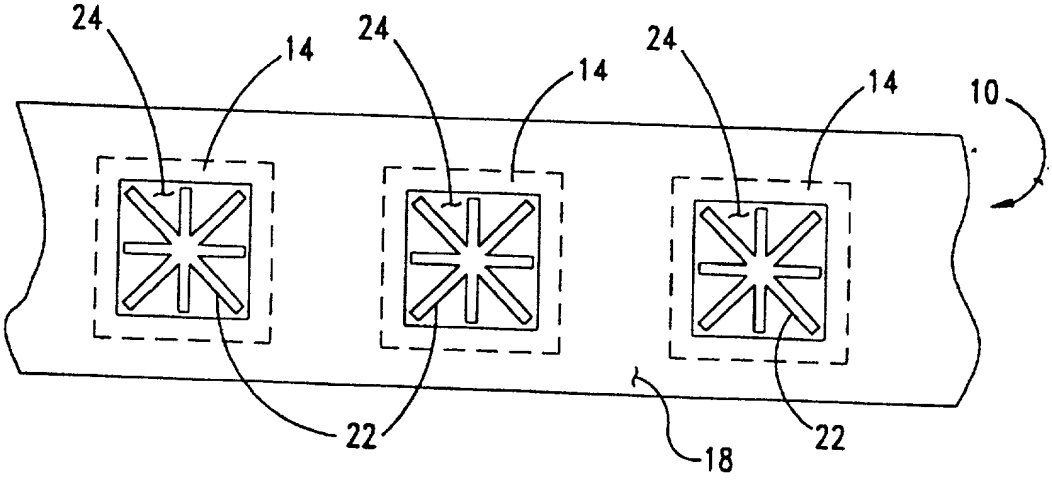

FIG. 4

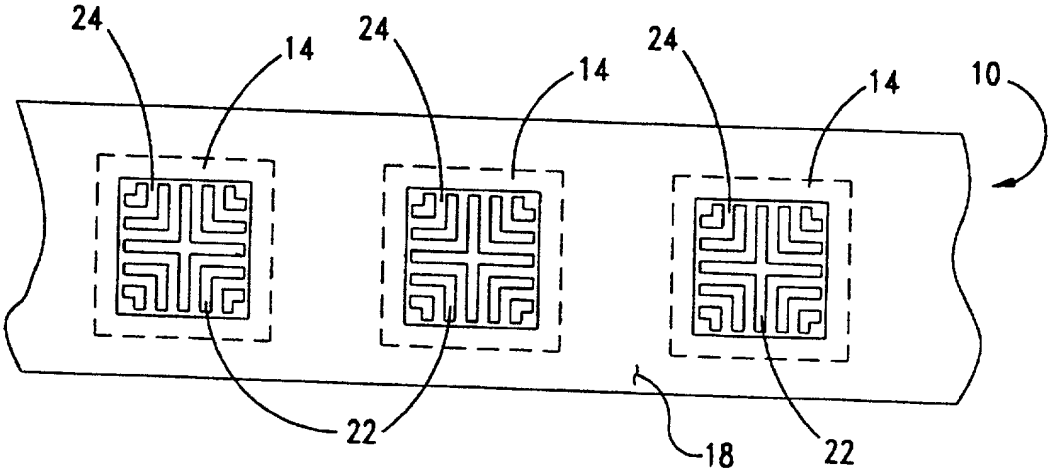

FIG. 5

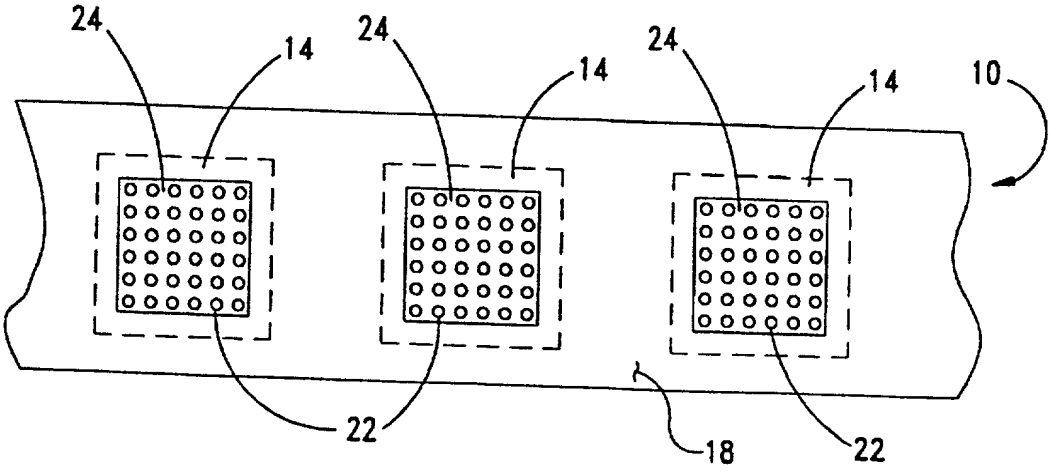

FIG. 6

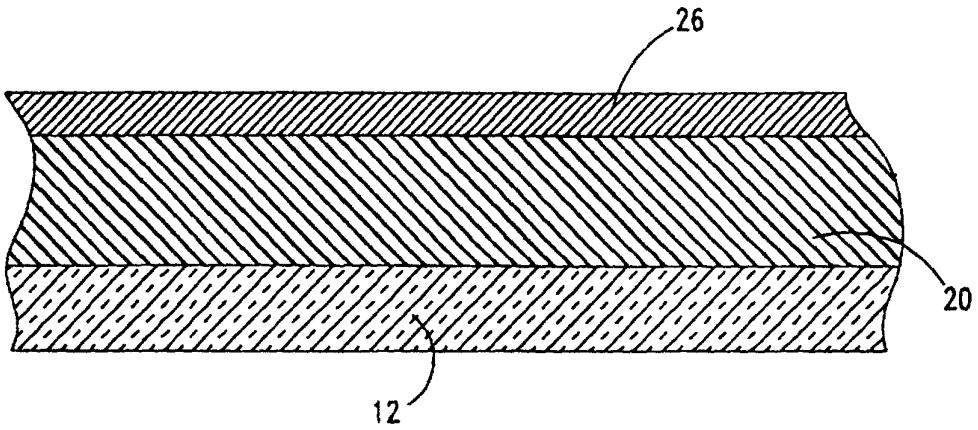

FIG. 7

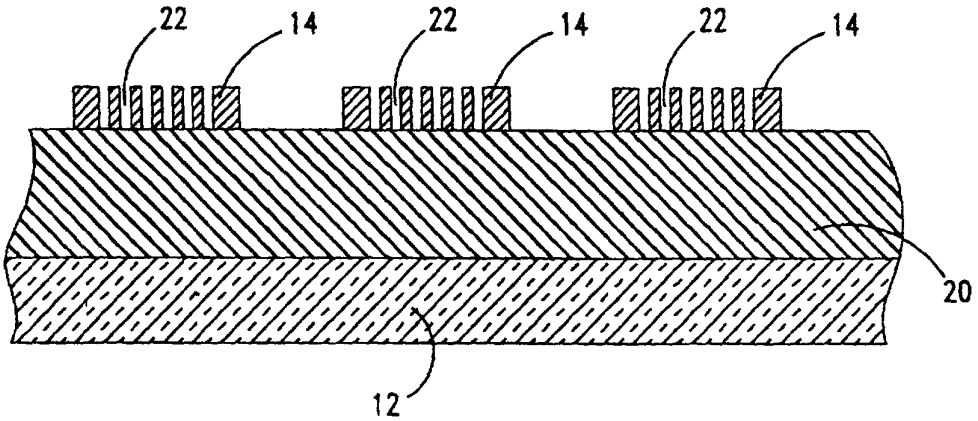

FIG. 8

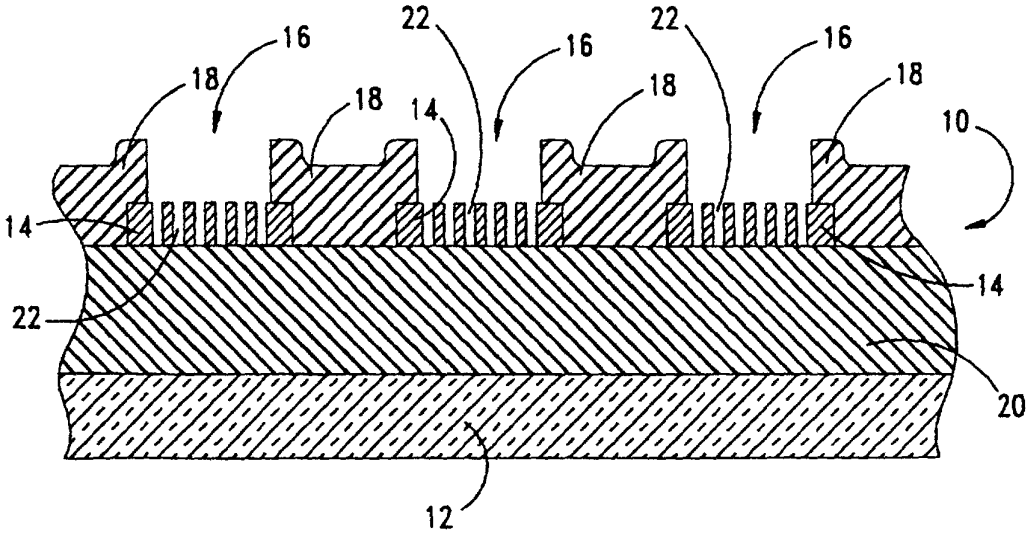

FIG. 9

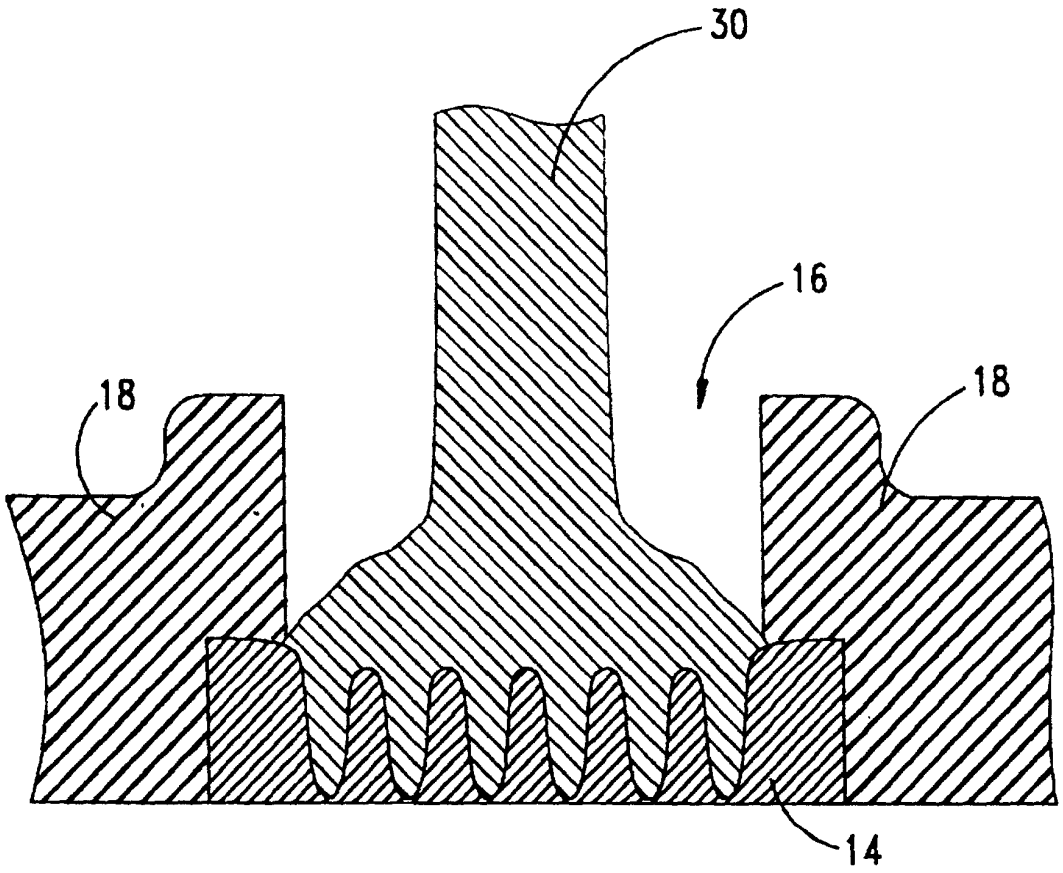

FIG. 10